REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow. Since this response has been filed within two (2) months after the February 12, 2004, mailing date of the Final Rejection in this application, a timely Advisory Action is requested.

In the February 12, 2004, Final Rejection, the Examiner rejected claims 77-81, 84 and 85 under 35 U.S.C. 103(a) as being unpatentable over the Igarishi et al. reference in view of the Lin reference and the Tsukamoto reference and the Kata et al. reference. Claim 82 was rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and Kata et al. and further in view of the Pasch reference. Claim 83 was rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and Kata et al. and further in view of the Knapp et al. reference.

The preamble of each of currently pending independent claims 77, 84 and 85 emphasizes that the claim is directed to a wafer scale structure. Moreover, each of the claims recites that the invention, as defined by each of these claims, includes a monolithic substrate of semiconductor material that is subdivided into a plurality of integrated circuit die regions and that each integrated circuit die region includes an integrated circuit formed in that region. As further recited in each of claims 77, 84 and 85, each of the integrated circuits formed in the plurality of integrated circuit die regions is substantially identical, since, as is well known, each of the circuits is typically formed utilizing a step-and-repeat procedure and an identical mask set.

Additionally, each of independent claims 77, 84 and 85 recites that the unitary, substantially planar prefabricated solid glass sheet utilized in the claimed wafer scale structure has a plurality of prefabricated hole formed therethrough and that the prefabricated holes are formed to provide a plurality of identical hole patterns, and that each hole pattern is identical to a corresponding pattern of die bond pads of the integrated circuits formed in the substrate wafer.

Each of claims 77, 84 and 85 further recites that an adhesive material disposed between the upper surface of the substrate wafer and the lower surface of the solid glass sheet affixes the solid glass sheet to the wafer substrate such that each pattern of prefabricated holes in the solid

glass sheet is aligned with an associated die bond pad pattern included in an associated integrated circuit structure formed in the substrate wafer.

Turning now to the Igarishi et al./Lin/Tsukamoto/Kata et al. reference combination cited by the Examiner against independent claims 77, 84 and 85, as previously submitted by Applicant, each of the Igarishi et al., Lin and Tsukamoto references is directed to a single integrated structure; that is, none of the references discusses structure at an earlier stage of the integrated circuit manufacturing process in which a plurality of integrated circuits are formed in a monolithic substrate wafer semiconductor material that has been subdivided into plurality integrated circuit die regions, wherein each integrated circuit die region includes a substantially identical integrated circuit structure. Furthermore, since none of these references is directed to a wafer scale structure, none of the references either teaches or suggests a unitary, substantially planar solid glass sheet having a plurality of prefabricated hole patterns formed therein so as to provide an association between each of the prefabricated hole patterns formed in the glass sheet and the corresponding conductive die bond pad pattern formed on each of the integrated circuits formed on the substrate wafer.

Essentially, Applicant submits that while each of the Igarishi et al., Lin and Tsukamoto references teaches a structure in which electrical connection is made to a pattern of die bond pads, none of the references, consider individually or in combination, either teaches or suggests a wafer scale structures that includes the physical features of a monolithic substrate wafer, a unitary, substantially planar prefabricated solid glass sheet, and an adhesive material disposed between the upper surface of the substrate wafer and the lower surface of the solid glass sheet to affix the solid glass sheet to the wafer to achieve alignment between the prefabricated hole patterns and the glass sheet and the die bond patterns on the semiconductor wafer substrate.

The Examiner now cites the Kara et al. reference in combination with the Igarishi et al., Lin and Tsukamoto references as suggesting the invention defined by Applicant's claims 77, 84 and 85. However, while Kata et al. do disclose a waferscale technology, the reference does not disclose a wafer scale structure that uses a substantially planar solid glass sheet that includes prefabricated hole patterns. Rather, as stated in the Kata al el. reference at, for example, column 4, lines 49-58:

"The wafer 10' is then provided with a passivating film 12. More particularly, the entire surface of the wafer 10' is covered with the passivating film 12. The passivating film 12 may be made of, for example, polyimide, silicon nitride, or silicon oxide by using a well-known technique such as spin coating. The passivating film has a thickness of 20 micrometers or smaller. After the formation of the passivating film, the chip electrodes are exposed to the atmosphere by means of exposing the wafer 10' to light and etching it."

Those skilled in art would clearly recognize that Kata et al. thus teaches, as evidenced by reference to the spin-coating technique, the covering of the wafer 10' with a liquid passivating layer, not the substantially planar solid glass sheet recited in claims 77, 84 and 85. Furthermore, Kata et al. expressly teaches that the chop elecrode holes are formed in the passivating film 12 after is formed on the surface of the wafer 10', in direct contrast to the prefabricated hole pattern recited in claims 77, 84 and 85.

For the reasons set forth above, Applicant submits that each of Applicant's independent claims 77, 84 and 85 patentably distinguishes over the Igarishi et al./Lin/Tsukamoto/Kata et al. reference combination.

Furthermore, since each of claims 79-83 depends directly from independent claim 77, Applicant submits that each of dependent claims 79-83 also patenably distinguishes over the cited reference combination.

For the reasons set forth above, Applicant is of the good faith belief that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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